FDN338P

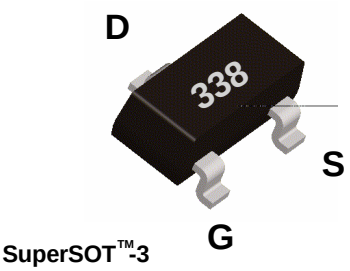
General Description

SuperSOT™-3 P-Channel logic level enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage applications in notebook computers, portable phones, PCMCIA cards, and other battery powered circuits where fast switching, and low in-line power loss are needed in a very small outline surface mount package.

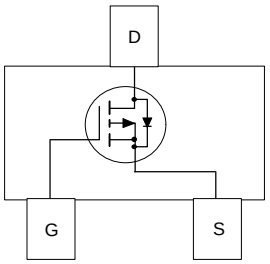
Features

- -1.6 A, -20 V, $R_{DS(ON)}$ = 0.13 Ω @ V_{GS} = -4.5 V
  $R_{DS(ON)}$ = 0.18 Ω @ V_{GS} = -2.5 V.
- Industry standard outline SOT-23 surface mount package using proprietary SuperSOT™-3 design for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.

SuperSOT™-3 | SuperSOT™-6 | SuperSOT™-8 | SO-8 | SOT-223 | SOIC-16



SuperSOT™-3



Absolute Maximum Ratings T_A = 25°C unless other wise noted

Symbol	Parameter	FDN338P	Units
V_{DSS}	Drain-Source Voltage	-20	V
V_{GSS}	Gate-Source Voltage - Continuous	±8	V
I_D	Drain/Output Current - Continuous	-1.6	A
	- Pulsed	-5	
P_D	Maximum Power Dissipation (Note 1a)	0.5	W
	(Note 1b)	0.46	
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150	°C
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	75	°C/W

Electrical Characteristics (T_A = 25 °C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-20			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25 °C		-28		mV/ °C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -16 V, V_{GS} = 0 V			-1	µA
		T_J = 55°C			-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V,V_{DS} = 0 V			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V			-100	nA
ON CHARACTERISTICS (Note)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-0.4	-0.6	-1	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	I_D = -250 µA, Referenced to 25 °C		2		mV/ °C
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = -4.5 V, I_D = -1.6 A		0.115	0.13	Ω
		T_J =125°C		0.16	0.22	
		V_{GS} = -2.5 V, I_D = -1.3 A		0.155	0.18	
$I_{D(ON)}$	On-State Drain Current	V_{GS} = -4.5 V, V_{DS} = -5 V	-2.5			A
g_{FS}	Forward Transconductance	V_{DS} = -5 V, I_D = -1.6 A		3		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz		405		pF
C_{oss}	Output Capacitance			170		pF
C_{rss}	Reverse Transfer Capacitance			45		pF
SWITCHING CHARACTERISTICS (Note)						
$t_{D(on)}$	Turn - On Delay Time	V_{DD} = -5 V, I_D = -1 A, V_{GS} = -4.5 V, R_{GEN} = 6 Ω		6.5	13	ns
t_r	Turn - On Rise Time			20	35	ns
$t_{D(off)}$	Turn - Off Delay Time			31	50	ns
t_f	Turn - Off Fall Time			21	35	ns
Q_g	Total Gate Charge	V_{DS} = -5 V, I_D = -1.6 A, V_{GS} = -4.5 V		6	8.5	nC
Q_{gs}	Gate-Source Charge			0.8		nC
Q_{gd}	Gate-Drain Charge			1.3		nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-0.42	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -0.42 A (Note)		-0.7	-1.2	V

Note:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Typical $R_{\theta JA}$ using the board layouts shown below on FR-4 PCB in a still air environment :

a. 250°C/W when mounted on 0.02 in² pad of 2oz Cu.

a

b. 270°C/W when mounted on a 0.001 in² pad of 2oz Cu.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300µs, Duty Cycle ≤ 2.0%.